Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	28	DIMM and inductor$1	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2006/01/08 11:19
L2	7	1 and SDRAM	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2006/01/08 11:12
L3	5	2 and interface	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2006/01/08 11:11
L4	7723	(transmission adj line$1) and inductor$1	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2006/01/08 11:19
L5	1394	4 and interface	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2006/01/08 11:19
L6	17	5 and SDRAM	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2006/01/08 11:21
L7	854	5 and resistor	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2006/01/08 11:21
L8	716	7 and impedance	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2006/01/08 11:21
L9	7	8 and DIMM	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2006/01/08 11:22
L10	13	(DIMM adj connector) and SDRAM	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2006/01/08 11:22
L11	2	10 and inductor	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2006/01/08 11:24
L12	375	7 and memory	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2006/01/08 11:24

L13	177	12 and transformer	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2006/01/08 11:25
L14	12	13 and SRAM	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2006/01/08 11:25
L15	1	13 and SDRAM	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2006/01/08 11:26
L16	2772	SDRAM and (memory adj controller)	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2006/01/08 11:26
L17	15	16 and inductor	USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2006/01/08 11:26